WHAT IS CLAIMED IS:

1. A method of encoding data words, the method comprising steps of:

(a) mapping a block of at least one of the data words into an error correction code (ECC) code word which is defined by a plurality of multiple-bit ECC symbols that are separated by boundaries; and

(b) constraining bit patterns from occurring in the ECC code word based on a relative location of the bit patterns to the boundaries.

2. The method of claim 1 wherein:

in step (a), each ECC symbol comprises a plurality of inner bit positions and a plurality of outer bit positions, which are closer to respective ones of the boundaries than the inner bit positions; and

in step (b), constraining the bit patterns comprises imposing different code constraints on the outer bit positions than on the inner bit positions to avoid selected bit patterns, which are allowed in the inner bit positions, from occurring in the outer bit positions.

3. The method of claim 1 wherein step (a) comprises:

(a)(1) encoding each data word into a data code word according to a code which constrains the bit patterns from occurring in the data code word based on a location of the bit patterns in the data code word relative to bit positions in the data code word that correspond to the boundaries between the multiple-bit ECC symbols; and

(a)(2) mapping a block of at least one of the data code words into a data field of the ECC code word, which comprises a first set of the ECC symbols.

4. The method of claim 3 wherein step (a) further comprises:

(a)(3) generating a second set of the ECC symbols, which are separated by boundaries, as a polynomial function of the first set of ECC symbols;

(a)(4) constraining the bit patterns from occurring in the second set of ECC symbols based on a relative location of the bit patterns to the boundaries of the second set of ECC symbols; and

(a)(5) mapping the second set of ECC symbols into an ECC field of the ECC code word.

5. The method of claim 1 wherein:

the bit patterns include bit patterns having three consecutive transitions between first and second binary states, wherein a middle one of the transitions occurs at one of the boundaries.

6. An encoder for encoding successive data words into respective, successive code words, the encoder comprising:

a data word input;

a code word output; and

a first encoder unit which maps each successive data word received on the data word input into a respective, successive code word on the code word output according to a first code, wherein the first code identifies in each code word boundaries between multiple-bit error correction code (ECC) symbols and imposes different code constraints on bit positions in each code word that are closer to the boundaries than bit positions in each code word that are farther from the boundaries.

7. The encoder of claim 6 and further comprising:

an ECC encoder which receives the successive code words from the first encoder unit and maps a block of at least one of the code words into a data field of an ECC code word and concatenates an ECC field onto the data field based on the data field and a predetermined ECC polynomial function, wherein the ECC code word is defined by a plurality of multiple-bit ECC symbols within the data field and the ECC field.

8. The encoder of claim 7 and further comprising:

a second encoder unit which maps each ECC symbol in the ECC field into an encoded ECC symbol according to a second code, wherein the second code identifies boundaries between the encoded ECC symbols in the ECC field and imposes different code constraints on bit positions in each encoded ECC symbol that are closer to the boundaries in the ECC field than bit positions that are farther from the boundaries in the ECC field.

9. The encoder of claim 8 wherein the first and second codes prevent selected bit patterns from occurring in the ECC code word, wherein the selected bit patterns include bit patterns having three consecutive transitions between first and second binary states with a middle one of the transitions occurring at one of the ECC symbol boundaries in the ECC code word.

10. A disc drive storage channel comprising:

a transducer capable of communicating with a data storage disc; and

encoding means coupled to the transducer for encoding data into successive error correction code (ECC) code words formed of multiple-bit ECC symbols according to a code, wherein the code

constrains bit patterns from occurring in each ECC code word based on a relative location of the bit patterns to boundaries between the multiple-bit ECC symbols, and for transmitting the ECC code words to the transducer as a code word stream.

11. A disc drive storage channel comprising:

a transducer capable of communicating with a data storage disc; and

decoding means coupled to the transducer for receiving a read signal from the transducer and for decoding successive error correction code (ECC) code words represented by the read signal into successive data words according to a code, wherein each ECC code word comprises a plurality of multiple-bit ECC symbols and the code constrains bit patterns in each ECC code word based on a relative location of the bit patterns to boundaries between the multiple-bit ECC symbols.